

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

C. Amendments to the Claims.

1. (Previously Presented) A semiconductor device structure on a silicon substrate, comprising:

5 a contact which penetrates an interlayer insulating film and is electrically connected with a diffusion layer in the silicon substrate;

a gate electrode which is formed on the silicon substrate and contains a nitride film at upper and side portions;

an insulating film formed from a gas containing carbon; and

10 a silicon nitride film for preventing carbon diffusion, having a portion sandwiched between the interlayer insulating film and the silicon substrate and adjacent to the gate electrode in a direction essentially parallel to a substrate surface, such a sandwiched portion having a thickness in a direction perpendicular to the substrate surface that is less than a thickness of the gate electrode in the perpendicular direction, the silicon nitride film traversing a region except a
15 portion for providing the electrical connection between the contact and the diffusion layer, and is formed on the nitride film at the upper and side portions of the gate electrode.

20 2. (Previously Presented) The semiconductor device according to claim 1, wherein:

the insulating film includes tantalum oxide (Ta_2O_5); and

the semiconductor device is a dynamic random access memory having a memory cell capacitor film including the tantalum oxide.

3. (Cancelled)

25 4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

7. (Withdrawn) A method for manufacturing a semiconductor device on a silicon substrate, having a device structure including an insulating film formed from gas containing carbon, comprising the step of:

forming a silicon nitride film between the insulating film and the silicon
5 substrate for preventing carbon from diffusing to the silicon substrate.

8. (Withdrawn) The method for manufacturing a semiconductor device of claim 7, further including the steps of:

forming a word line on a silicon substrate;

forming the silicon nitride film over the entire surface of the substrate

10 including the word line;

forming a first interlayer insulating film on the silicon nitride film;

etching the first interlayer insulating film to form a cell contact hole with
an etching method selective for the silicon nitride film to expose the silicon nitride
film at a bottom of the cell contact hole;

15 selectively etching the silicon nitride film exposed at the bottom of the cell
contact hole to expose the silicon substrate; and

forming a cell contact plug in the cell contact hole.

9. (Withdrawn) The method for manufacturing a semiconductor device of claim 8, further including the steps of:

20 forming a first capacitor electrode electrically connected to the cell contact
plug;

forming the insulating film; and

forming a second capacitor electrode on the insulating film.

10. (Withdrawn) The method for manufacturing a semiconductor device of claim 9, wherein:

25 the insulating film includes tantalum oxide (Ta_2O_5).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

11. (Withdrawn) The method for manufacturing a semiconductor device of claim 7, further including the steps of:

forming a word line on a silicon substrate;

forming a first interlayer insulating film on the silicon substrate including
5 the word line;

forming a cell contact plug through the first interlayer insulating film to
provide an electrical connection with a diffusion layer in the silicon substrate;

forming a second interlayer insulating film on the first interlayer insulating
film;

10 forming a bit line on the second interlayer insulating film;

forming a third interlayer insulating film on the second interlayer
insulating film including the bit line;

forming a capacitor contact plug through the second and third interlayer
insulating films to provide an electrical connection to the cell contact plug; and

15 forming the silicon nitride film on the third interlayer insulating film and
capacitor contact plug.

12. (Withdrawn) The method for manufacturing a semiconductor device of claim 11, further including the steps of:

forming a fourth interlayer insulating film on the silicon nitride film;

20 forming a capacitor formation section in the fourth interlayer insulating
film to expose the silicon nitride film; and

etching the exposed silicon nitride film to expose the capacitor contact
plug.

13. (Withdrawn) The method for manufacturing a semiconductor device of claim 12, further
25 including the step of:

forming a capacitor including the insulating film in the capacitor
formation section.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

14. (Withdrawn) The method for manufacturing a semiconductor device of claim 7, further including the steps of:

forming a word line on a silicon substrate;

forming a first interlayer insulating film on the silicon substrate including
5 the word line;

forming a cell contact plug through the first interlayer insulating film to
provide an electrical connection with a diffusion layer in the silicon substrate;

forming a second interlayer insulating film on the first interlayer insulating
film;

10 forming a bit line on the second interlayer insulating film;

forming a third interlayer insulating film on the second interlayer
insulating film including the bit line;

forming the silicon nitride film on the third interlayer insulating film; and

forming a capacitor contact plug through the second and third interlayer
15 insulating films and the silicon nitride film to provide an electrical connection to
the cell contact plug.

15. (Withdrawn) The method for manufacturing a semiconductor device of claim 14, further including the step of:

forming a capacitor including the insulating film and having a capacitor
20 electrode electrically connected to the capacitor contact plug.

16. (Withdrawn) The method for manufacturing a semiconductor device of claim 7, further including the steps of:

forming a word line on a silicon substrate;

forming a first interlayer insulating film on the silicon substrate including
25 the word line;

forming a cell contact plug through the first interlayer insulating film to
provide an electrical connection with a diffusion layer in the silicon substrate;

forming a second interlayer insulating film on the first interlayer insulating
film;

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

forming a bit line on the second interlayer insulating film;
forming the silicon nitride film on the second interlayer insulating film
including the bit line;
forming a third interlayer insulating film on the silicon nitride film;
5 etching the third interlayer insulating film to form a contact hole and
expose the silicon nitride film at a bottom of the contact hole;
etching the silicon nitride film at the bottom of the contact hole to expose
the second interlayer insulating film;
etching the exposed second interlayer insulating film at the bottom of the
10 contact hole to provide a capacitor contact hole including the contact hole; and
forming a capacitor contact plug through the second and third interlayer
insulating films to provide an electrical connection to the cell contact plug.

17. (Withdrawn) The method for manufacturing a semiconductor device of claim 16, further
including the step of:

15 forming a capacitor including the insulating film and having a capacitor
electrode electrically connected to the capacitor contact plug.

18. (Withdrawn) A method for manufacturing a semiconductor device on a silicon substrate,
having a memory cell including a capacitor insulating film formed from gas containing carbon,
comprising the step of:

20 forming a silicon nitride film between the capacitor insulating film and the
silicon substrate for preventing carbon from diffusing to the silicon substrate.

19. (Withdrawn) The method of manufacturing the semiconductor device of claim 18, wherein:
the capacitor insulating film includes tantalum oxide (Ta_2O_5).

20. (Withdrawn) The method of manufacturing the semiconductor device of claim 19, wherein:
25 the capacitor includes an electrode having a hemi-spherical grain structure.

21. (Currently Amended) A semiconductor device on a silicon substrate, having a device

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

structure including an insulating film formed from gas containing carbon, comprising:

a contact which penetrates a first interlayer insulating film and is electrically connected with a diffusion layer in the silicon substrate;

a capacitor contact that is interposed between a lower electrode of a memory cell capacitor and the contact while penetrating a second interlayer insulating film and a third interlayer insulating film;

a conductor which is formed on the second interlayer insulating film and below at least a portion of the third interlayer insulating film, and that contains a nitride film at upper and side portions, the side portion nitride film in direct contact with the capacitor contact and the conductor **and not in contact with the third interlayer insulating film;**

a fourth interlayer insulating film which is formed on the third interlayer insulating film;

a silicon nitride film for preventing carbon diffusion, having a portion sandwiched between the fourth interlayer insulating film and the third interlayer insulating film while traversing a region except a connection portion between the lower electrode and the capacitor contact, and is formed above the nitride film at the upper portion of the conductor.

22. (Previously Presented) The semiconductor device according to claim 21, wherein:

the insulating film includes tantalum oxide (Ta_2O_5); and

the semiconductor device is a dynamic random access memory having a memory cell capacitor film including the tantalum oxide.

23. (Currently Amended) A semiconductor device on a silicon substrate, having a device structure including an insulating film formed from gas containing carbon, comprising:

a contact that is electrically connected with a diffusion layer formed in the silicon substrate while penetrating a first interlayer insulating film, the contact is electrically connected to a capacitor contact that is interposed between a lower electrode of a memory cell capacitor and the contact while penetrating a second interlayer insulating film and a third interlayer insulating film for providing an

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

electrical connection between the lower electrode and the contact;

a conductor which is formed on the second interlayer insulating film and below at least a portion of the third interlayer insulating film, and that contains a nitride film at upper and side portions;

5 a silicon nitride film for preventing carbon diffusion, which is formed between the second and third interlayer insulating film **and that extends over the second interlayer insulating film in a lateral direction with a vertical thickness less than that of the conductor** while traversing a region except a connection portion between the lower electrode and the capacitor contact, and is
10 formed on the nitride film at the upper and side portions of the conductor.

24. (Previously Presented) The semiconductor device according to claim 23, wherein:

the insulating film includes tantalum oxide (Ta_2O_5); and

the semiconductor device is a dynamic random access memory having a
15 memory cell capacitor film including the tantalum oxide.

25. (Previously Presented) The semiconductor device according to claim 1, wherein:

the silicon nitride film for preventing carbon diffusion includes a portion having a bottom surface in contact with and extending parallel to the diffusion
20 layer away from the gate electrode and a top surface in contact with an interlayer insulating film.